

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

5     Patent No.:    US 7,345,365 B2                      Issue Date:    03/18/2008  
     Serial No.:    10/728,150                      Filing Date:    12/03/2003  
     Inventor:       Jin-Yuan Lee et al.  
     Docket No.:    MEGP0012USA1

10           Title:    ELECTRONIC COMPONENT WITH DIE AND PASSIVE DEVICE

To:                    Commissioner for Patents  
                         P.O. BOX 1450  
                         Alexandria, VA 22313-1450

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Subject:            Request for Certificate of Correction of Office Mistake

Dear Sir:

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The above-identified patent was issued on 03/18/2008. The applicants found that the Related U.S. Application Data and Foreign Application Priority Data were missed on the front page of the patent (Attachment 1). Documents on record indicate this as an Office mistake of consequence.

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The patent is a divisional application of, and claims the priority benefit of, U.S. application serial No. 10/055,499 filed on 01/22/2002. The Related U.S. Application Data listed on the specification submitted on 12/03/2003 (Attachment 2) and the Office Action of 07/06/2004 pointed out the PTO had received the priority documents. (Attachment 3, PTOL-326, page 2)

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The applicants submitted priority document and claimed for foreign priority on 12/03/2003. Both of the declaration (Attachment 4) and the specification (Attachment 5) submitted on 12/03/2003 indicate that the PTO received the submission of priority

document and claimed for foreign priority on 12/03/2003.

The applicants hereby request that a Certificate of Correction be issued under 37 CFR 1.322 to supplement the Related U.S. Application Data (Division of application No. 10/055,499, filed on 01/22/2002) and the Foreign Application  
5 Priority Data (Taiwan patent application No. 90133093 dated 12/31/2001).

Sincerely yours,

\_\_\_\_\_/Winston Hsu/

Date: \_\_\_\_\_02/26/2009

10 Winston Hsu, Patent Agent No. 41,526  
P.O. BOX 506, Merrifield, VA 22116, U.S.A.  
Voice Mail: 302-729-1562  
Facsimile: 806-498-6673  
e-mail : winstonhsu@naipo.com

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7345365  
APPLICATION NO.: 10/728,150  
ISSUE DATE : 3/18/2008  
INVENTOR(S) : Jin-Yuan Lee et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

### On Title Page

Under item (65), Insert item (62) "Related U.S. Application Data," and add--Division of application No. 10/055,499, filed on Jan. 22, 2002.--

Under item (62), Insert item (30) "Foreign Application Priority Data," and add--Dec. 31, 2001 (TW)  
-----90133093 A--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*



US007345365B2

(12) **United States Patent**  
**Lee et al.**

(10) **Patent No.:** **US 7,345,365 B2**  
(45) **Date of Patent:** **Mar. 18, 2008**

(54) **ELECTRONIC COMPONENT WITH DIE AND PASSIVE DEVICE**

(75) Inventors: **Jin-Yuan Lee**, Hsinchu (TW);  
**Mou-Shiung Lin**, Hsinchu (TW);  
**Ching-Cheng Huang**, Hsinchu (TW)  
(73) Assignee: **MEGICA Corporation**, Hsinchu (TW)  
(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/728,150**

(22) Filed: **Dec. 3, 2003**

(65) **Prior Publication Data**

US 2004/0119097 A1 Jun. 24, 2004

(51) **Int. Cl.**  
**H01L 23/52** (2006.01)  
**H01L 23/48** (2006.01)  
**H01L 23/40** (2006.01)  
**H01L 23/34** (2006.01)  
**H01L 23/538** (2006.01)  
(52) **U.S. Cl.** ..... **257/724; 257/723; 257/774; 257/E23.174; 257/E23.177**  
(58) **Field of Classification Search** ..... **257/723-724, 257/700, 774, 781, 698, E23.174, E23.177**  
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,402,888 A \* 9/1983 Runck ..... 264/448

5,049,980 A \* 9/1991 Saito et al. .... 257/758  
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\* cited by examiner

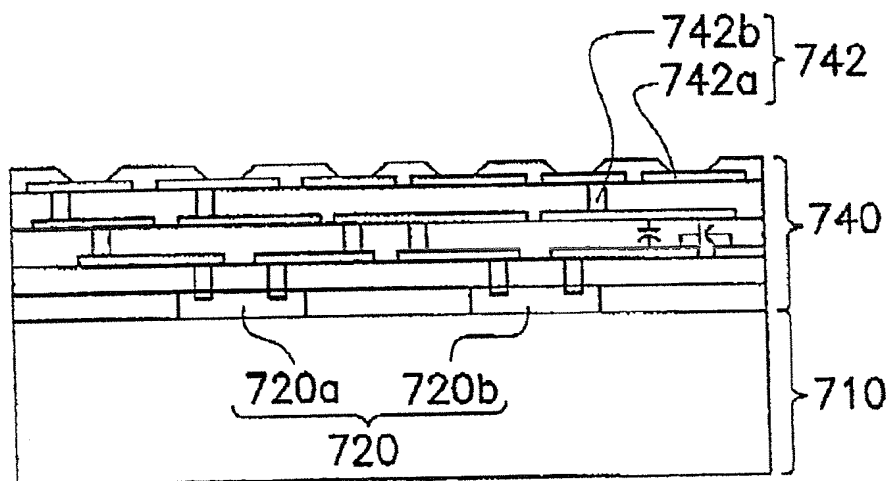
Primary Examiner—Luan Thai

(74) Attorney, Agent, or Firm—Winston Hsu

(57) **ABSTRACT**

An integrated chip package structure and method of manufacturing the same is by adhering dies on an organic substrate and forming a thin-film circuit layer on top of the dies and the organic substrate. Wherein the thin-film circuit layer has an external circuitry, which is electrically connected to the metal pads of the dies, that extends to a region outside the active surface of the dies for fanning out the metal pads of the dies. Furthermore, a plurality of active devices and an internal circuitry is located on the active surface of the dies. Signal for the active devices are transmitted through the internal circuitry to the external circuitry and from the external circuitry through the internal circuitry back to other active devices. Moreover, the chip package structure allows multiple dies with different functions to be packaged into an integrated package and electrically connecting the dies by the external circuitry.

34 Claims, 17 Drawing Sheets



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Please supply the Related U.S. Application Data (Division of application No. 10/055,499, filed on 01/22/2002)

Please supply the Foreign Application Priority Data (Taiwan patent application No. 90133093 dated 12/31/2001)

PATENT

Docket No.:JCLA8534-D

**In The Specification:**

Paragraph beginning at line 7 of page 1 has been amended as follows:

~~This application claims the priority benefit of Taiwan application serial no: 90133093, filed December 31, 2001. This application is a divisional application of, and~~  
claims the priority benefit of, U.S. application serial No. 10/055,499 filed on January 22, 2002.

**Office Action Summary**

Application No.

10/728,150

Applicant(s)

LEE ET AL.

Examiner

Luan Thai

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-60 and 176-203 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 1-60 and 176-203 are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 10/055,499.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

0000 [5486 ON X8/X1] 92:91 NOW 20/12/10

P534

## COMBINED DECLARATION AND POWER OF ATTORNEY

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name and that I believe I am an original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**INTEGRATED CHIP PACKAGE STRUCTURE USING ORGANIC SUBSTRATE AND  
METHOD OF MANUFACTURING THE SAME**

the specification of which

X is attached hereto.

— was filed on \_\_\_\_\_  
as Application Serial No. \_\_\_\_\_ and was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Date Filed(yyyy/mm/dd)	Yes	No
90133093	Taiwan, R.O.C.	2001/12/31	X	

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Jiawei Huang	(Reg. No. 43,330)	Charles C.H. Wu	(Reg. No. 39,081)
Maria Erlinda C. Sarno	(Reg. No. 37,436)	Chanette Armstrong	(Reg. No. 44,011)
Belinda Lee	(Reg. No. 46,863)		

SEND CORRESPONDENCE TO:

DIRECT TELEPHONE CALLS TO:  
(Name and telephone number)

J.C. Patents, Inc.  
4 Venture, Suite 250,  
Irvine, CA 92618  
(949) 660-0761

Jiawei Huang  
(949) 660-0762

INTEGRATED CHIP PACKAGE STRUCTURE USING ORGANIC SUBSTRATE  
AND  
METHOD OF MANUFACTURING THE SAME

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CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90133093, filed December 31, 2001.

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BACKGROUND OF THE INVENTION

Field of the invention:

[0001] The present invention relates to an integrated chip package structure and method of manufacture the same. More particularly, the present invention relates to an integrated chip package structure and method of manufacture the same using organic  
15 substrate.

Description of related art

[0002] In the recent years, the development of advanced technology is on the cutting edge. As a result, high-technology electronics manufacturing industries launch